What is claimed is:

1. A method, comprising:

dividing an oscillating signal having a first frequency according to a sequence of divide ratios to produce a divided signal having a frequency approximating a reference signal frequency; and

adapting said first frequency to reduce a phase difference between said divided signal and said reference signal;

wherein a next value in said sequence of divide ratios is determined by (a) accumulating an error between a present value in said sequence of divide ratios and an average value of said sequence of divide ratios, (b) accumulating the accumulated errors, and (c) selecting the next value in said sequence of divide ratios such that the multiply-accumulated error values are maintained within finite bounds.

2. The method of claim 1, further comprising filtering a control signal to remove high-frequency phase noise prior to using said control signal for adapting said first frequency to reduce a phase difference between said divided signal and said reference signal.

3. The method of claim 1, wherein the multiply-accumulated error is fed back to a first means of at least two means for accumulating.

4. A phase-locked loop-type frequency synthesizer comprising:

a reference signal source for providing a reference signal having a first frequency;

a programmable oscillator for providing an oscillating signal having a second frequency;

a programmable pre-scaler for dividing the oscillating signal from said programmable oscillator according to a sequence of divide ratios to produce a divided signal having a frequency approximating the reference signal frequency;

a phase comparator for a) comparing said divided signal and said reference signal, b) determining, if any, a phase difference between said divided

signal and said reference signal and c) generating a control signal for adapting said programmable oscillator to reduce a phase difference between said divided signal and said reference signal; and

a modulator for providing said sequence of divide ratios wherein a next value in said sequence of divide ratios is provided by (a) accumulating an error between a present value in said sequence of divide ratios and an average value of said sequence of divide ratios, (b) accumulating the accumulated errors, and (c) selecting the next value in said sequence of divide ratios such that the multiply-accumulated error values are maintained within finite bounds, wherein said modulator comprises:

a first accumulator for accumulating an error between a present value in said sequence of divide ratios and an average value of said sequence of divide ratios;

a second accumulator for accumulating an error output of said first accumulator; and

a feedback circuit comprising at least said first accumulator and said second accumulator for feeding back an accumulated error to the first accumulator for providing a next value in said sequence of divide ratios.

5. The synthesizer of claim 4, wherein said reference frequency has a frequency equal to f*M and said programmable oscillator has a frequency equal to f*N and the sequence of divide ratios comprises an integer sequence having an average value substantially equal to N/M.

6. The synthesizer of claim 5, wherein both N and M are programmable.

7. The synthesizer of claim 6, wherein N and M may be reprogrammed during operation.

8. The synthesizer of claim 4, wherein said programmable oscillator comprises a voltage controlled oscillator.

9. The synthesizer of claim 4, further comprising a filter for filtering said control signal to remove high-frequency phase noise prior to adapting said programmable oscillator.

10. The synthesizer of claim 9, wherein said filter comprises a loop filter.

11. The synthesizer of claim 4, further comprising a summing circuit interposed between said modulator output and an input to said pre-scaler for offsetting the sequence of divide ratios determined by said modulator, such that said sequence of divide ratios may contain values beyond those which may be represented in the modulator.

12. The synthesizer of claim 4, wherein only said pre-scaler is required to operate at the full frequency of said programmable oscillator.

13. The synthesizer of claim 4, wherein said pre-scaler provides a clock signal for the modulator.

14. The synthesizer of claim 4, wherein said modulator further comprises at least a third accumulator for accumulating a phase error output of a previous accumulator.

15. The synthesizer of claim 4, wherein the accumulators of said modulator comprise carry chains.

16. The synthesizer of claim 15, wherein at least a portion of the feedback circuit is delayed to allow for pipelining of said carry chains.

17. The synthesizer of claim 4, wherein said feedback circuit further comprises at least one summing circuit and a numeric divider circuit adapted to determine a next value in the sequence of divide ratios needed to maintain said accumulators finite and without overflow.

18. The synthesizer of claim 17 wherein said numeric divider circuit produces an approximation of an ideal quotient.

19. A modulator for producing an integer sequence with an average value of N/M, wherein N and M are integers, comprising:

a first accumulator for accumulating an error between said integer sequence and said average value, N/M;

a second accumulator for accumulating an error output of said first accumulator; and

a feedback circuit comprising at least said first accumulator and said second accumulator for feeding back an accumulated error to the first accumulator for providing a next value in said integer sequence such that the multiply-accumulated error values are maintained within finite bounds.

20. The modulator of claim 19, wherein both N and M are programmable.

21. The modulator of claim 20, wherein N and M may be programmed during operation.

22. The modulator of claim 19, further comprising at least a third accumulator for accumulating an error output of a previous accumulator.

23. The modulator of claim 19, wherein said accumulators of said modulator comprise carry chains.

24. The modulator of claim 23, wherein at least a portion of the feedback circuit is delayed to allow for pipelining of said carry chains.

25. The modulator of claim 19, wherein said feedback circuit further comprises at least one summing circuit and a numeric divider circuit adapted to determine a next value in said integer sequence needed to maintain said accumulators finite and without overflow.

26. The modulator of claim 25 wherein said numeric divider circuit produces an approximation of an ideal quotient.

27. A method for reducing phase noise, comprising:

clocking a programmable pre-scaler using the frequency output of a voltage controlled oscillator;

dividing the frequency output of said voltage controlled oscillator in said pre-scaler using a divide ratio sequence to form an approximation frequency that is on average substantially equal to a reference signal, said divide ratio sequence having an average value substantially equal to N/M, wherein N and M are integers;

comparing the phases of said approximation frequency and said reference signal; and

in response to a difference in phase between said approximation frequency and said reference signal, generating a control signal to adjust the frequency output of said voltage controlled oscillator to correct for the difference;

wherein only said pre-scaler is required to operate at the full frequency of said voltage controlled oscillator; and

wherein a modulator provides the divide ratio sequence to said pre-scaler to be used for the dividing of the frequency output of said voltage controlled oscillator, said modulator comprising:

a first accumulator for accumulating an error between said divide ratio sequence and said average value, N/M;

a second accumulator for accumulating an error output of said first accumulator; and

a feedback circuit for feeding back an accumulated error to the first accumulator for providing a next value in said sequence of divide ratios such that the multiply-accumulated error values are maintained within finite bounds.